RESTATEMENT OF THE CLAIMS

1. (Previously Presented) A video signal control circuit receiving a video signal including a plurality of lines each of which nominally includes a standard number of pixels as an input data, the video signal control circuit comprising:

a delay circuit delaying the input data with a plurality of delay times so that the delay circuit outputs a plurality of delayed input data;

a counter circuit that counts a pixel number of each line in the input data; and

a judgment circuit that calculates a difference between the standard number and the pixel number counted by the counter circuit, and outputs a calculated difference signal; and

a selector combining the delayed input data in response to the calculated difference signal to generate as an output data, combined input data having the standard number of pixels.

2. (Previously Presented) A video signal control circuit as claimed in Claim 1, wherein the delay circuit includes a plurality of flip-flop circuits converting the input data into the delayed input data with each delayed by one clock.

3. (Cancelled)

4. (Original) A video signal control circuit as claimed in Claim 1, wherein the judgment circuit is able to set an initial value of the delay to the delay circuit in accordance with a selection signal.

5. (Original) A video signal control circuit as claimed in Claim 4, further comprising an initial value judgment circuit that judges an inclination of a pixel dispersion on the basis of the pixel number counted by the counter circuit, and outputs the selection signal that designates an initial delay in accordance with the inclination of the pixel dispersion.

6. (Previously Presented) A video signal control circuit receiving a video signal including a plurality of lines each of which nominally includes a standard number of pixels as an input data, the video signal control circuit comprising:

a memory circuit which the input data can be written in and read from, which includes two one-port memories, wherein the input data are alternately written in the two one-port memories, and the written input data are alternately read from the two one-port memories;

an address generation circuit that outputs a write address or a read address to the memory circuit;

a counter circuit that counts a pixel number of each line in the input data; ~~and~~

a judgment circuit that calculates a difference between the standard pixel number and the pixel number counted by the counter circuit, and calculates a new address value in accordance with an address value generated by the address generation circuit and the calculated difference; and

an output selector combining the input data read from the memory circuit based on the new address to generate as an output data, combined input data having the standard number of pixels.

7. (Previously Presented) A video signal control circuit that processes a video signal of which one line is composed of plural pixels as an input data, comprising:

a memory circuit including a two-port memory that is able to write in and read out the input data in parallel;

an address generation circuit that outputs a write address or a read address to the memory circuit;

a counter circuit that counts a pixel number of each line in the input data; and

a judgment circuit that calculates a difference between a set standard pixel number and the pixel number counted by the counter circuit, and calculates a new address value in accordance with an address value generated by the address generation circuit and a delay signal on the basis of the calculated difference;

wherein the address generation circuit generates the write address or the read address on the basis of the address value and the delay signal calculated by the judgment

circuit, and when there is a difference between the pixel number of the input data read from the memory circuit and that of the input data written in the memory circuit, some of the plural read addresses each corresponding to the plural data to be read are repeated or deleted, in accordance with the difference between the pixel numbers, the input data read from the memory circuit according to the plural read addresses constituting an output data of the video signal control circuit.

8-9. (Cancelled)

10. (Original) A video signal control circuit as claimed in Claim 6, wherein the judgment circuit is able to set an initial value of the address generated by the address generation circuit in accordance with a selection signal.

11. (Original) A video signal control circuit as claimed in Claim 10, further comprising an initial value judgment circuit that judges an inclination of a pixel dispersion on the basis of the pixel number counted by the counter circuit, and outputs the selection signal that designates an initial value of the address in accordance with the inclination of the pixel dispersion.

12. (Original) A video signal control circuit as claimed in Claim 7, wherein the judgment circuit is able to set an initial value of the address generated by the address generation circuit in accordance with a selection signal.

13. (Original) A video signal control circuit as claimed in Claim 12, further comprising an initial value judgment circuit that judges an inclination of a pixel dispersion on the basis of the pixel number counted by the counter circuit, and outputs the selection signal that designates an initial value of the address in accordance with the inclination of the pixel dispersion.

14. (Previously Presented) A video signal control circuit as claimed in Claim 6, wherein the address generating circuit includes a plurality of address counters.

15. (Previously Presented) A video signal control circuit as claimed in Claim 7, wherein the address generating circuit includes a plurality of address counters.

16. (Previously Presented) A video signal control circuit as claimed in Claim 1, wherein the counter circuit counts the pixel number of each line in the input data in response to a horizontal synchronous signal received by the counter circuit.

17. (Previously Presented) A video signal control circuit as claimed in Claim 6, wherein the counter circuit counts the pixel number of each line in the input data in response to a horizontal synchronous signal received by the counter circuit.

18. (Previously Presented) A video signal control circuit as claimed in Claim 7, wherein the counter circuit counts the pixel number of each line in the input data in response to a horizontal synchronous signal received by the counter circuit.